A Schmitt Trigger by means of Complimentary Pass Transistor Logic

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Abstract— ***The current paper presents a Schmitt trigger circuit based on Complementary Pass Transistor Logic (CPTL). The hysteresis curves of proposed Schmitt trigger is presented, hysteresis width depends on supply voltage and transistor geometry. The performance of the proposed circuit is examined using Cadence and the model parameters of gpdk-180 nm CMOS process. Simulation results are presented. The Schmitt trigger layout is presented with optimized sizing and spacing in compliance to the design rules of gpdk-180 nm CMOS process.***

I. INTRODUCTION

The Schmitt trigger is a circuit used extensively in both the analog and digital circuits. The Schmitt trigger is a comparator circuit that incorporates positive feedback. When the input is higher than a certain chosen threshold, the output is high; when the input is lower than the other chosen threshold, the output is low and when the input is mediating the two, the output retains its value. The trigger is so designated because the output retains its value until the input changes sufficiently to trigger a change [1-6]. Several methods have been proposed to implement Schmitt trigger. However sizing up the Schmitt triggers (to rise and fall times of signals) increases layout area and power dissipation. It is well known that CMOS Schmitt triggers are the circuits that convert a varying voltage in to a stable logical signal [7-10]. They have been used extensively to improve on/off control and reduce the sensitivity to noise or disturbances. If noise magnitude of the input signal is less than switching threshold difference, Schmitt trigger will not respond, thus making the later immune to undesired noise. Schmitt trigger circuit has been widely used in the input buffers to increase noise immunity. Several Schmitt trigger circuits had been reported for different applications [11-25].

In this paper, we present a Schmitt trigger circuit based on complementary pass transistor logic. The remaining sections of the paper are structured as follows. The proposed circuit description is presented in section II. Simulation results are included in section III. Finally, conclusions are included in section IV.

II. CIRCUIT DESCRIPTION

Figure 1 depicts the schematic diagram of CPTL inverter circuit. The CPTL uses series transistors to select between possible inverted output values of the logic, the output of which drives an inverter to generate the non-inverted output signal. Inverted and non-inverted inputs are needed to drive the gates of the pass-transistors. The main advantages are full swing, elimination of static power in the inverter through level restorer and pass transistor. Since restorer is only active when the input V_i is high. The level restoration transistor improves capacitance; takes away pull down current at point *'p'* strife between level restoration transistor and input transistor (slower switching). Hence level restoration transistor is also to be sized to its minimum level. Feedback inverter and level restoration transistor are also to be sized such that the voltage at node *'p'* drops below the threshold of the inverter, which carries function in the sizes of output inverter.

The new proposed Schmitt trigger is shown in Fig 2. It is comprised of two Complementary Pass Transistor Logic (CPTL) Inverters ($CPTL_1$ consists of M_1-U_1-U_2) and ($CPTL_2$ consists of M_2-U_3-U_4) and two output MOS transistors (M_3 - M_4).

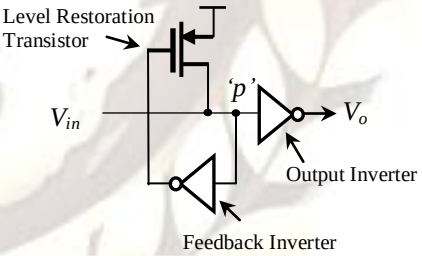

Fig. 1 CPTL Inverter circuit

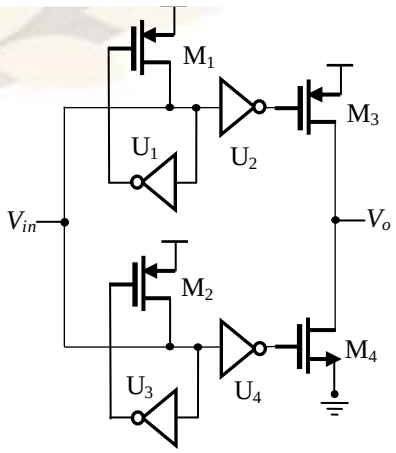

Fig. 2 New proposed Schmitt trigger circuit

When no input signal is given, outputs of $CPTL_1$ and $CPTL_2$ are ON thereby M_3 is OFF and M_4 is ON. And the resultant output voltage is V_{out} = 0 V. It is assumed that, input V_{in} is positive rising triangular waveform. When the input voltage V_{in} is greater than threshold voltage V_{th}, outputs of $CPTL_1$ and $CPTL_2$ are OFF and thus M_3 is ON and M_4 is OFF hence V_{out} is positive (i.e., supply rail voltage 2 V). This point is called UTP. The output voltage V_{out} remains positive until the input waveform reaches a value of less than V_{th}. when input voltage V_{in} is less than V_{th}, the outputs of $CPTL_1$ and $CPTL_2$ are ON thereby M_3 is OFF and M_4 is ON and hence V_{out}=0 V. This point is called LTP. The output voltage V_{out} remains zero until the input waveform voltage reaches a value of voltage greater than V_{th}. The cycle repeats and generates a square waveform as shown in the figure 3.

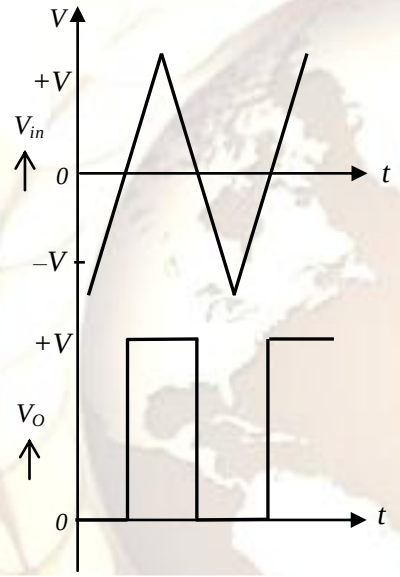

Fig. 3. Input/output waveforms of the proposed trigger circuit

III. SIMULATION RESULTS

The proposed circuit is designed and analyzed using Cadence gpdk 180 nm CMOS technology. The new proposed CPTL based Schmitt trigger shown in Fig. 2 is simulated and its input and output results are shown in Fig. 4.

The proposed Schmitt trigger circuit with high to low and low to high transition threshold voltages has better noise immunity than the inverter. As input signal V_{in} goes up to V_{DD} from GND, the threshold voltages of the proposed Schmitt trigger circuit is $V_{H.}$ Similarly as input signal V_{in} comes down to GND from V_{DD}, the threshold voltages of the proposed Schmitt trigger circuit is V_L. In other words, output signal V_o is pulled up as signal V_{in} is lower than V_L. Hence the noise immunity of the proposed Schmitt trigger circuit is better than that of inverter.

The circuit in Fig. 2 was tested for temperature stability ranging from –150°C to +150°C and the simulation profile produced to be less than 0.0003% variation in the case of square waveform. Figure 5 presents the temperature sensitivity of the proposed configuration. Simulated total power dissipation of the circuit is 28 pW.

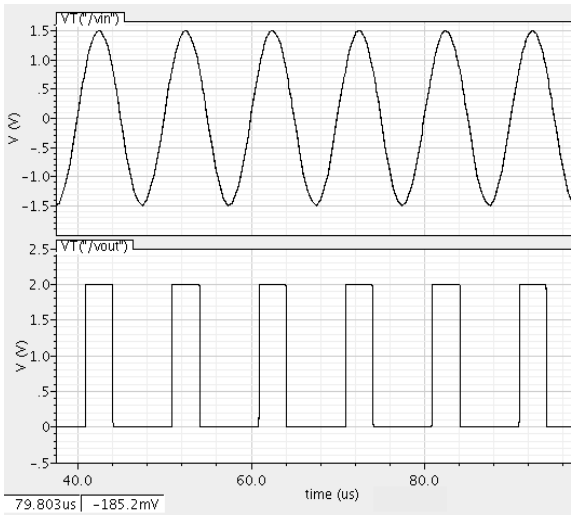

Fig. 4 Input and output waveforms of the Schmitt Trigger

Hysteresis curve shown in Fig. 6 is plotted using TSMC 180 nm CMOS technology process with 2 V supply voltage.

The Schmitt trigger layout is laid out with optimized sizing and spacing in compliance to the design rules of gpdk-180 nm CMOS process. The values of length and width and overall area of the proposed circuits are listed in table 1 and designed layout is shown in Fig. 7. The overall area occupied by the Complementary Pass Transistor Logic (CPTL) based Schmitt trigger is 148.58 μm^2.

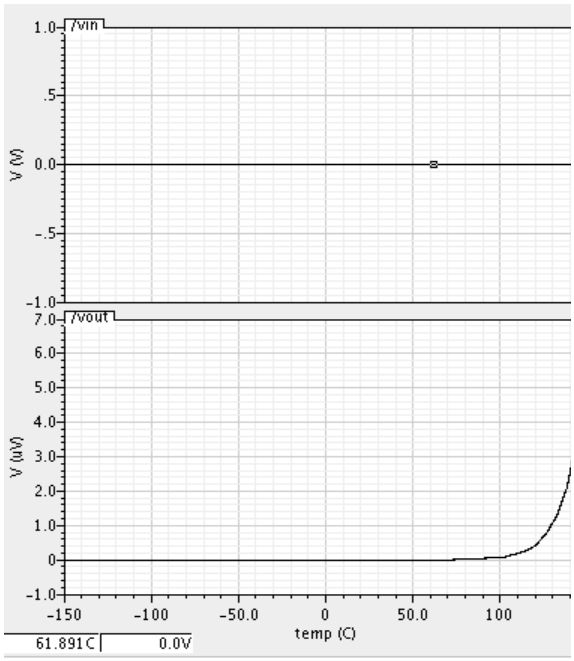

Fig. 5 Temperature sensitivity
(above: input sine wave and below: output square wave)

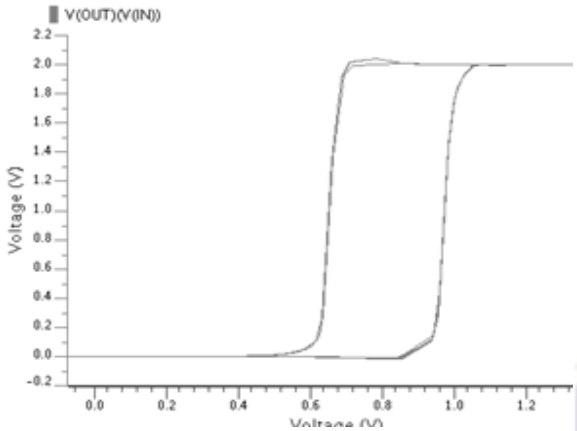

Fig. 6 Hysteresis curve of CPTL based Schmitt trigger

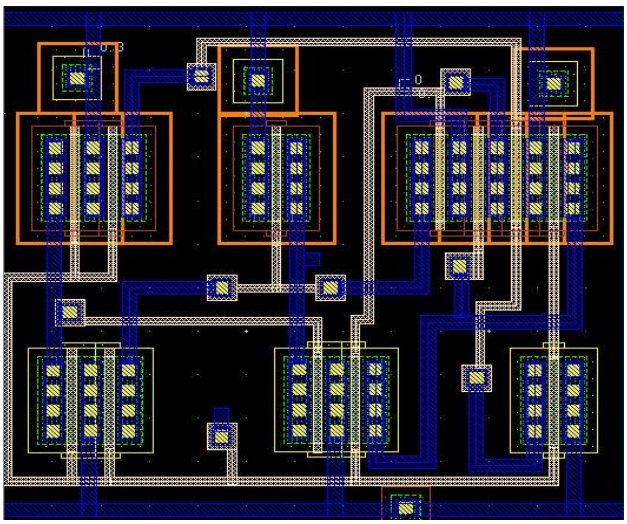

Fig. 7 Layout of the proposed CPTL based Schmitt trigger circuit

IV. CONCLUSION

A new CPTL based Schmitt trigger circuit, which has been realized using 180 nm CMOS technology is proposed and its characteristics have been quantified both analytically and numerically. The hysteresis feature is clear and less sensitive to the process and supply voltage variations compared to other CMOS Schmitt trigger. The new proposed Schmitt trigger circuit is suitable to reject noise for mixed voltage interface applications. The Schmitt trigger circuit described in this paper can be used as basic circuit for making more complex logic circuits with hysteresis transfer characteristics. The circuit may gain greater importance as it is bestowed with wider applications in many electronics and communication systems.

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